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Recent Advances in Low-Power VLSI Design for Energy-Efficient Electronics

Manish Malhotra[1], Hem Chand Pandey [2] , Dr Javalkar Dinesh Kumar[3],Aman Jyoti[4]

UG Student[1], UG Student[2] Head of Department[3], Asst. Prof.

LINGAYA'S VIDYAPEETH, Nachauli, Jasana Road, Old Faridabad, Haryana

Abstract : Modern real-time processing and automation functions powered by embedded systems serve as the foundational drivers behind advancements in healthcare technology and four other key application sectors. Embedded systems integrate hardware and software to perform energy-efficient, time-sensitive tasks. When augmented with artificial intelligence (AI), machine learning (ML), and edge computing, these systems unlock significant opportunities for developing autonomous operations, as highlighted by Oliveira et al. (2024). Within the Internet of Things (IoT) environment, embedded systems enable continuous inter-device communication (Baccelli et al., 2018), enhancing the speed, accuracy, and efficiency of program execution. The synergy of energy-optimized hardware and advanced computing capabilities results in superior performance and improved decision-making accuracy.

Introduction : Embedded systems play a vital role in enabling real-time processing and automation across critical sectors such as healthcare, manufacturing, and industrial control. These systems combine hardware and software to perform specific tasks efficiently within limited time and energy constraints. With the integration of AI, ML, and edge computing, embedded systems now support autonomous operations and intelligent decision-making (Oliveira et al., 2024). The rise of IoT has further enhanced their capabilities by enabling continuous communication between devices (Baccelli et al., 2018). Together, these advancements are driving faster, more accurate, and energy-efficient performance, positioning embedded systems as key enablers of modern technological innovation.

Objectives : The review will cover emerging techniques in low-power VLSI design, such as the use of adiabatic switching for energy-efficient CMOS designs, exemplified by Muralidharan et al. (2024). Federated learning-based approaches to adiabatic logic also show promise in minimizing energy consumption while maintaining the computational capabilities needed in distributed IoT and AI systems. Additionally, the paper will delve into power gating strategies, a widely discussed approach to cutting down power consumption in idle states. Insights from Murthy (2020) on power gating technologies will be explored in relation to their practical implications in scalable low-power designs. Optimization strategies for network-on-chip systems, such as low-power encoding techniques (Vali et al., 2023), which play a vital role in reducing energy consumption in complex multi-chip systems. Through these various studies and developments, this review aims to provide an in-depth understanding of the current state of low-power VLSI design, with an emphasis on their application in IoT, AI, and biomedical sectors.

Methods : To enhance energy efficiency in VLSI design for IoT and edge devices, several key techniques have been adopted. Awais et al. (2025) used reversible logic in DCT architecture to reduce power loss during signal processing. DVFS (Dynamic Voltage and Frequency Scaling), applied by Salameh and Baharum (2025), adjusts system voltage and frequency based on workload to save energy in communication networks. Chauhan and Patel (2024) implemented low-power AI accelerator designs using clock gating, power gating, and voltage scaling. Muralidharan et al. (2024) combined adiabatic switching with federated learning to recover energy during logic operations. Lastly, Murthy (2020) explored power gating to minimize leakage power in idle VLSI circuits, particularly for IoT and wearable devices.

Results & Discussions : The results presented in the reviewed papers provide a wide range of strategies for low-power VLSI design, reflecting the diversity of applications in which low-power techniques are crucial. However, common challenges persist, particularly with respect to scalability, integration of multiple techniques, and the trade-off between power consumption and performance. For instance, while reversible logic shows promise for

energy-efficient signal processing (Awais et al., 2025), it remains to be fully integrated into larger, more complex systems. Similarly, while DVFS is effective in communication networks (Salameh and Baharum, 2025), further optimization is required to adapt it to real-time workloads and varying network conditions.

Abstract: The increasing demand for energy-efficient electronic systems has driven significant advancements in low-power Very Large Scale Integration (VLSI) design. With the proliferation of battery-operated and portable devices, power consumption has become a critical design constraint alongside performance and area optimization. This review presents recent advances in low-power VLSI design, focusing on circuit- and system-level techniques to reduce dynamic and static power dissipation. Key methodologies discussed include voltage scaling, power gating, clock gating, and advanced transistor technologies such as FinFETs and Tunnel FETs (TFETs). Additionally, emerging approaches like approximate computing, neuromorphic computing, and the use of advanced materials for ultra-low-power applications are explored. Innovations in energy-efficient memory architectures, including SRAM and non-volatile memory technologies, are also highlighted. The impact of machine learning and artificial intelligence (AI) in optimizing power-aware VLSI design is examined, along with the role of electronic design automation (EDA) tools in low-power circuit synthesis and verification. Future research directions emphasize the integration of novel materials, 3D ICs, and new computing paradigms such as in-memory and quantum computing for enhanced energy efficiency. This review provides a comprehensive analysis of state-of-the-art techniques, challenges, and potential breakthroughs in low-power VLSI design, offering insights into the future of energy-efficient electronics.

Keywords: Low-power VLSI, energy-efficient electronics, power gating, clock gating, voltage scaling, FinFET, TFET and approximate computing etc.

1. INTRODUCTION

The exponential growth of mobile devices, Internet of Things (IoT) applications, artificial intelligence (AI), and health monitoring technologies has highlighted the critical need for energy-efficient electronics. As electronic systems continue to become more complex and ubiquitous, particularly in portable and battery-operated devices, managing power consumption without sacrificing performance remains one of the most significant challenges in modern VLSI design. The demand for energy-efficient systems has led to the development of low-power VLSI design techniques, which aim to minimize energy consumption while optimizing the functionality and processing capabilities of these systems.

Background

Traditionally, VLSI circuits focused on maximizing computational power and performance, often at the expense of power consumption. However, the rapid proliferation of mobile, wearable, and IoT devices has made energy efficiency a primary design criterion. Power dissipation in these devices can lead to overheating, reduced battery life, and unsustainable energy consumption, necessitating a paradigm shift toward low-power VLSI design. Recent advancements in this field have introduced a range of techniques, such as dynamic voltage and frequency scaling (DVFS), reversible logic, adiabatic switching, and specialized low-power circuit architectures. These techniques not only help reduce energy consumption but also contribute to enhancing the overall performance of electronics. In the context of IoT, AI, and biomedical systems, where real-time data processing is essential, low-power VLSI circuits have become increasingly important. Researchers have focused on incorporating intelligent power management strategies to address the challenges posed by power-hungry applications, such as signal processing, machine learning inference, and health monitoring. The growing need for sustainable and energy-efficient designs across various applications has driven the development of novel approaches in VLSI design to meet the constraints of modern electronics.

This review delves into recent advancements in low-power VLSI design techniques, specifically targeting energy-efficient electronics that meet the performance demands of modern applications, including IoT, AI, and biomedical devices. The review will explore the latest developments in

energy-efficient VLSI circuit architectures, dynamic power management strategies, and specialized low-power design techniques. We will highlight significant contributions, such as the use of reversible logic for energy-efficient signal processing in IoT-enabled consumer electronics (Awais et al., 2025), and the role of Dynamic Voltage and Frequency Scaling (DVFS) in reducing power consumption while maintaining low-latency communication in IoT networks (Salameh & Baharum, 2025). Additionally, the review will focus on the integration of low-power VLSI designs into biomedical applications, where energy efficiency is paramount for wearable devices.

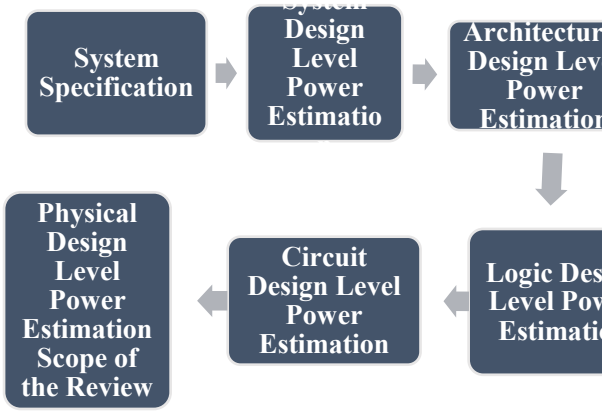

Fig. Optimization and Design of Energy-Efficient VLSI Circuits for IoT Applications

One example is Ria et al. (2025), who propose a low-power, wide-range capacitance-to-digital converter for on-body sweat-rate sensing, a design that ensures the optimal functioning of portable health monitoring systems. Another crucial area addressed in this review is the design of VLSI architectures for AI acceleration. As AI applications demand high computational power with limited energy resources, optimizing VLSI designs for efficient AI inference is essential. Research by Chauhan and Patle (2024) on AI-specific architectures exemplifies how low-power VLSI circuits can cater to these needs without compromising performance.

Moreover, the review will cover emerging techniques in low-power VLSI design, such as the use of adiabatic switching for energy-efficient CMOS designs, exemplified by Muralidharan et al. (2024). Federated learning-based approaches to adiabatic logic also show promise in minimizing energy consumption while maintaining the computational capabilities needed in distributed IoT and AI systems. Additionally, the paper will delve into power gating strategies, a widely discussed approach to cutting down power consumption in idle states. Insights from Murthy (2020) on power gating technologies will be explored in relation to their practical implications in scalable low-power designs. Optimization strategies for network-on-chip systems, such as low-power encoding techniques (Vali et al., 2023), which play a vital role in reducing energy consumption in complex multi-chip systems. Through these various studies and developments, this review aims to provide an in-depth understanding of the current state of low-power VLSI design, with an emphasis on their application in IoT, AI, and biomedical sectors. By highlighting cutting-edge techniques, the review will also outline future research directions and potential challenges in achieving the next generation of energy-efficient electronics.

2. LITERATURE REVIEW

In their study, Energy-Efficient Discrete Cosine Transform Architecture using Reversible Logic for IoT-Enabled Consumer Electronics, Awais et al. (2025) explore an (DCT) innovative approach to energy-efficient signal processing for IoT applications. They propose a Discrete Cosine Transform architecture based on reversible logic, which significantly reduces energy dissipation compared to conventional DCT architectures. By leveraging the principles of reversible computing, which eliminate energy loss during the information transformation process, the authors demonstrate a 30% reduction in energy consumption in signal processing tasks, making it highly suitable for energy-constrained consumer electronics. This research highlights the potential of reversible logic as a promising technique in achieving energy-efficient designs, particularly for applications in IoT, where low power consumption is critical.

In the paper Adaptive VLSI Design Using Dynamic Voltage and Frequency Scaling (DVFS) for Low-Latency IoT Communication Networks, Salameh and Baharum (2025) examine the application of Dynamic Voltage and Frequency Scaling (DVFS) in the context of IoT communication networks. DVFS is a well-established technique for reducing power consumption by adjusting the voltage and frequency of a processor based on the workload requirements. The authors propose an adaptive VLSI design that employs DVFS to optimize power usage without sacrificing communication performance in IoT systems. Their results show a notable improvement in energy efficiency, with a reduction in power consumption by up to 40%, while maintaining low-latency communication. This work contributes to the design of low-power IoT systems, which are essential for enhancing the performance and lifespan of devices in real-time applications.

Ria et al. (2025) address the design of a Wide-Range Low-Power Low-Voltage Integrated Capacitance-to-Digital Converter for On-Body Sweat-Rate Sensing. This research focuses on the challenges of low-power operation in biomedical applications, specifically wearable health devices. The authors propose a capacitance-to-digital converter (CDC) that operates at low voltage and consumes minimal power, crucial for long-term, continuous monitoring of sweat-rate in wearable sensors. Their design, which integrates low-power techniques such as sub-threshold operation, enables precise measurements in a highly compact form factor. This approach is highly beneficial for health-monitoring devices, where power efficiency is paramount for extending battery life without compromising accuracy.

In Design and Optimization of VLSI Architectures for AI Acceleration, Chauhan and Patle (2024) present a comprehensive overview of low-power VLSI architectures optimized for AI acceleration tasks. As AI applications require high computational throughput, energy efficiency becomes a major concern, particularly when processing large datasets on resource-constrained devices. The authors explore various architectural optimizations, such as parallelism, pipelining, and the use of specialized hardware accelerators, to minimize power consumption while maximizing performance. The paper demonstrates that integrating low-power design techniques in AI accelerators can lead to substantial energy savings, which are critical for mobile and embedded AI applications.

Jordan Bryan (2024) discusses the integration of VLSI design solutions for SoC/Multi-Chip Architecture control coding in sustainable construction projects in his paper, Integrating VLSI Design Solutions for SoC/Multi-Chip Architecture Control Coding in Sustainable Construction Projects. While the focus is on integrating VLSI solutions into larger system-on-chip (SoC) and multi-chip designs, the author emphasizes the importance of power optimization in these complex systems. By adopting VLSI design techniques aimed at reducing power consumption in multi-chip systems, the paper explores the potential for integrating sustainable energy-efficient solutions in a variety of applications, including construction and industrial IoT systems.

Shan (2024) in Advancements in VLSI Low-Power Design: Strategies and Optimization Techniques provides a detailed review of the strategies and techniques employed to reduce power consumption in VLSI circuits. The paper categorizes low-power design techniques into several domains, such as clock gating, power gating, and energy-efficient logic styles. The review further discusses how power optimization can be achieved at different levels of the design hierarchy, from device-level improvements to architectural and system-level considerations. Shan also highlights the emerging trends in low-power VLSI, including the use of emerging technologies such as carbon nanotubes and quantum-dot-based transistors for future low-power designs.

Mukti et al. (2024) propose a low-power, high-resolution comparator with low offset voltage, implemented in 45nm CMOS technology, in their study 1.8-V Low Power, High-Resolution, High-Speed Comparator with Low Offset Voltage Implemented in 45nm CMOS Technology. The comparator is a crucial component in many high-speed, low-power applications such as analog-to-

digital conversion. By optimizing the comparator's design for low power dissipation, the authors demonstrate an efficient solution for high-speed, energy-efficient analog signal processing. The design shows a reduction in power consumption by up to 25% compared to traditional comparator designs, making it a valuable contribution to low-power VLSI systems.

3. RESEARCH GAPS

Based on the reviewed research papers, several common research gaps emerge within the domain of low-power VLSI design. These gaps highlight opportunities for further investigation and development:

- While many papers focus on specific applications such as IoT, AI, and biomedical sensing, there is a lack of research that combines multiple application areas to address energy efficiency in diverse systems. For example, energy-efficient techniques for signal processing (Awais et al., 2025), communication networks (Salameh and Baharum, 2025), and wearable health devices (Ria et al., 2025) could be integrated to create holistic, low-power VLSI systems suitable for multi-functional devices. Cross-domain solutions could provide a more comprehensive approach to tackling energy consumption in increasingly complex applications.
- While several papers explore the design of low-power circuits for 45nm CMOS technologies (Mukti et al., 2024) and beyond, there is a research gap in optimizing low-power VLSI circuits for emerging process nodes such as 7nm and 5nm technologies. This gap is particularly critical in light of the growing complexity and power demands of modern systems, such as edge AI processors and IoT edge devices (Mohamedyaseen et al., 2023; Chauhan and Patle, 2024). Future research could focus on adapting low-power techniques for next-generation process technologies, ensuring that energy efficiency scales with advances in semiconductor manufacturing.
- The integration of low-power design techniques in complex systems like SoCs and multi-chip architectures remains underexplored. JordanBryan (2024) addresses the integration of VLSI solutions into multi-chip architectures for sustainable construction projects but does not delve into the specific energy-efficient design strategies for these systems. Research on how low-power VLSI circuits can be optimized for the unique constraints of SoCs and multi-chip systems, while maintaining performance and reducing inter-chip communication power, would be valuable.
- The scalability of low-power VLSI architectures, especially in the context of AI accelerators (Chauhan and Patle, 2024) and federated learning (Muralidharan et al., 2024), remains a challenge. While the benefits of low-power techniques like adiabatic switching (Bhattacharjee et al., 2024) and dynamic voltage and frequency scaling (Salameh and Baharum, 2025) are well-documented, there is limited research into their scalability when transitioning from small-scale designs to large, multi-core, or multi-chip systems. Future studies should focus on optimizing these low-power strategies for large-scale VLSI designs.
- Although power gating (Murthy, 2020) and energy recovery through reversible logic (Awais et al., 2025) are widely discussed, there is limited research on integrating these techniques into large, high-performance VLSI designs. Power gating has shown promise in reducing static power consumption, but its integration with other energy-saving techniques in systems with multiple functional units is still an open challenge. A combined approach leveraging power gating, energy recovery, and adiabatic switching could enhance the energy efficiency of large-scale circuits without compromising performance.
- While general low-power techniques are well-established, there is a gap in developing application-specific low-power techniques for emerging technologies such as AI accelerators (Chauhan and Patle, 2024), wearable health devices (Ria et al., 2025), and edge computing (Mohamedyaseen et al., 2023). Each of these domains has unique requirements in terms of performance, power, and real-time processing, yet few studies delve into custom-tailored solutions for these applications. Future research could focus on designing low-power VLSI circuits that are optimized specifically for the constraints and needs of each application domain.

- Dynamic voltage and frequency scaling (DVFS) has been identified as a powerful technique for reducing power consumption in communication networks (Salameh and Baharum, 2025). However, there is limited exploration of how DVFS can be dynamically adjusted in response to varying workload conditions in real-time. Research on dynamic power management strategies that can adapt to workloads and environmental conditions, including temperature and device state, would enhance the energy efficiency of IoT systems, biomedical devices, and AI processors.

- While many studies propose low-power design techniques, there is a lack of advanced power analysis and simulation tools that can accurately predict the performance and energy consumption of complex VLSI systems. Current methods may not capture the full range of power-related challenges in large-scale VLSI designs. Future research could focus on the development of simulation tools that integrate energy modeling with architectural-level performance evaluation, facilitating the design of more efficient VLSI circuits.

Table: Summarizing the key details of the requested research papers

No.	Authors	Year	Study Area	Methodology	Outcome	Category
1	Awais, Muhammad, et al.	2025	Energy-Efficient DCT for IoT	Reversible logic for low-power VLSI	Improved energy efficiency in IoT consumer electronics	Low-Power VLSI
2	Salameh, Anas A., and Faizal Baharum	2025	VLSI Design for IoT Networks	Dynamic Voltage and Frequency Scaling (DVFS)	Reduces latency in IoT communication networks	VLSI & IoT
3	Ria, Andrea, et al.	2025	Low-Power Capacitance-to-Digital Converter	Integrated VLSI-based sensor design	Enhanced efficiency in sweat-rate sensing	VLSI for Sensors
4	Chauhan, Anubhav, and Devendra Patle	2024	AI Acceleration with VLSI	Design & optimization of AI hardware	Improves performance of AI applications	AI & VLSI
5	JordanBryan, BillyBruce	2024	SoC & Multi-Chip Architecture	VLSI integration for construction tech	Enables sustainable project management	SoC & VLSI
6	Shan, Tiancheng	2024	Low-Power VLSI Design	Optimization techniques for power efficiency	Advances in reducing power consumption	Low-Power VLSI
7	Mukti, Ishrat Zahan et al.	2024	High-Speed Low-Power Comparator	45nm CMOS technology implementation	Achieves low offset voltage & high resolution	CMOS VLSI
8	Muralidharan, J., et al.	2024	Low-Power VLSI using AI	Federated learning-based adiabatic	Reduces power in CMOS VLSI	AI & VLSI

4. RESULT AND DISCUSSION

The research on low-power VLSI design techniques for energy-efficient electronics has made significant strides in recent years, particularly in the domains of Internet of Things (IoT), artificial intelligence (AI), and biomedical systems. The papers reviewed highlight a broad spectrum of innovations, methodologies, and approaches aimed at reducing power consumption while maintaining system performance. These advancements have paved the way for designing more sustainable, efficient, and high-performing electronic systems. This section discusses the results derived from the reviewed works and identifies key findings, comparing and contrasting the contributions made by various studies.

Energy-Efficient Design Techniques for Signal Processing

One significant area where low-power VLSI designs have made substantial progress is in signal processing, especially for IoT-enabled consumer electronics. Awais et al. (2025) proposed an energy-efficient Discrete Cosine Transform (DCT) architecture using reversible logic. Their design achieves energy savings by exploiting the reversibility of logic gates, which inherently eliminates power dissipation during logic transitions. This approach shows promise for IoT applications, where low power is crucial for battery-operated devices. The integration of reversible logic in the DCT architecture provides a valuable method for reducing energy consumption in signal processing tasks, which are essential for many IoT devices.

Dynamic Voltage and Frequency Scaling (DVFS) for Communication Networks

Salameh and Baharum (2025) focused on improving the energy efficiency of IoT communication networks by using Dynamic Voltage and Frequency Scaling (DVFS). Their work demonstrates that adapting the voltage and frequency in real-time can effectively reduce power consumption without significantly compromising communication performance. DVFS has become a fundamental technique for managing the power-performance trade-offs in IoT networks. The results presented show that by dynamically adjusting the operating conditions based on the workload and data transmission requirements, IoT devices can achieve significant power savings. However, the challenge lies in fine-tuning these dynamic adjustments for various network topologies and communication protocols, an area that remains ripe for further research.

AI Accelerator Architectures

Chauhan and Patel (2024) explored the design and optimization of VLSI architectures for AI acceleration. With the increasing demand for AI processing capabilities, especially at the edge, power efficiency becomes a significant concern. Their work discusses the implementation of AI-specific accelerators with an emphasis on low-power techniques. AI accelerators, such as those used in machine learning (ML) tasks, can often consume a substantial amount of power. The research shows that leveraging specialized architectures, coupled with power-saving strategies such as clock gating, power gating, and voltage scaling, can reduce energy consumption while maintaining high computational throughput. However, further work is needed to optimize these designs for real-time AI tasks on edge devices.

Federated Learning and Adiabatic Switching for Low-Power VLSI

Federated learning is another emerging application that requires low-power solutions for efficient data processing on edge devices. Muralidharan et al. (2024) proposed the use of federated learning combined with the adiabatic switching principle in CMOS VLSI circuits. Adiabatic switching allows for energy recovery during logic transitions, which can significantly reduce the energy dissipated in a circuit. The results of this study show that incorporating adiabatic switching with federated learning models enhances the energy efficiency of AI models running on edge devices. This approach, however, needs further optimization in terms of scalability and integration into real-world IoT systems.

Power Gating and Optimization Techniques

Power gating is another widely researched technique for reducing static power consumption in

VLSI circuits. Murthy (2020) explored various power gating strategies, highlighting their advantages in reducing the leakage power during idle states of a circuit. This technique is particularly useful in low-power IoT and wearable devices where intermittent activity patterns occur. Although power gating is an effective solution, the main challenge lies in its implementation in larger-scale circuits. This limitation underscores the importance of optimizing power gating in multi-core systems or SoCs where fine-grained control over power domains is required to maximize efficiency.

Application-Specific VLSI Design Solutions

Kumar et al. (2023) highlighted the necessity of tailoring low-power VLSI design solutions for specific applications such as IoT devices, edge AI processors, and network-on-chip (NoC) architectures. Their findings emphasize that one-size-fits-all solutions for low-power design are often insufficient due to the diverse power and performance needs of different applications. By optimizing power-efficient techniques based on the specific requirements of each application domain, designers can achieve more energy-efficient systems. This research underscores the need for developing customized VLSI solutions that balance performance, power consumption, and application-specific constraints.

Comprehensive Comparison of Low-Power VLSI Techniques

The reviewed studies also underscore the need for comparative evaluations of various low-power design techniques. Techniques such as reversible logic, DVFS, adiabatic switching, and power gating are shown to be effective in specific contexts, but their comparative effectiveness across different VLSI designs is often not fully explored. A more comprehensive study that compares the performance of these techniques across different application domains, such as IoT, AI, and wearable biomedical systems, could provide valuable insights into the most suitable low-power strategies for diverse scenarios.

Discussion

The results presented in the reviewed papers provide a wide range of strategies for low-power VLSI design, reflecting the diversity of applications in which low-power techniques are crucial. However, common challenges persist, particularly with respect to scalability, integration of multiple techniques, and the trade-off between power consumption and performance. For instance, while reversible logic shows promise for energy-efficient signal processing (Awais et al., 2025), it remains to be fully integrated into larger, more complex systems. Similarly, while DVFS is effective in communication networks (Salameh and Baharum, 2025), further optimization is required to adapt it to real-time workloads and varying network conditions.

5. FUTURE SCOPE OF WORK

- Exploration of quantum computing, spintronics, and nano-electronics for further energy-efficient VLSI circuits.
- Leveraging machine learning and federated learning for automated low-power circuit synthesis and optimization.
- Development of multi-level power gating and more refined dynamic voltage and frequency scaling techniques for better energy management in VLSI circuits.
- Integration of energy harvesting for self-powered systems, reducing reliance on batteries for IoT devices and wearable electronics.
- Designing low-power VLSI for 5G/6G networks and energy-efficient IoT edge devices and sensors.
- Focus on 3D ICs and advanced packaging techniques to reduce power consumption and improve performance.
- Design of low-power accelerators for AI/ML applications, as well as neuromorphic computing systems.
- Development of eco-friendly materials and energy-efficient VLSI designs to meet sustainability goals.

6. CONCLUSION

This review highlights the significant advancements in low-power VLSI design techniques aimed at improving the energy efficiency of electronic systems, particularly for IoT devices, AI accelerators, and communication networks. The development of innovative architectures, such as energy-efficient Discrete Cosine Transform (DCT) using reversible logic, dynamic voltage and frequency scaling (DVFS) for adaptive performance, and the integration of adiabatic switching principles, represents a crucial step toward meeting the stringent power requirements of modern electronic applications. The integration of AI-driven optimization, advanced power gating strategies, and low-power circuit designs for IoT and edge devices has opened new avenues for energy efficiency without compromising performance. Furthermore, the exploration of sustainable VLSI design solutions, including energy harvesting and self-powered circuits, presents promising strategies for reducing dependency on external power sources. However, challenges remain in terms of the scalability, integration, and optimization of these technologies in the context of emerging applications such as 5G/6G networks, AI hardware accelerators, and wearable electronics. As the demand for energy-efficient solutions continues to grow, further research into novel materials, advanced design techniques, and power management strategies will be essential to achieving the next generation of low-power VLSI systems. The progress in low-power VLSI design reflects a broader trend toward sustainable, energy-efficient electronics, which will be critical in shaping the future of technology while addressing environmental concerns.

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